VLSI TITLES 2015-2016

FIR FILTER:

1. A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications
2. An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis
3. Optimal Factoring of FIR Filters
4. Exact and Approximate Algorithms for the Filter Design Optimization Problem
5. Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System
6. An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC
7. Fault Tolerant Parallel Filters Based on Error Correction Codes
8. Array-Based Approximate Arithmetic Computing: A General Model and Applications to Multiplier and Squarer Design
9. High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations
10. Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block
11. An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability
12. Investigation of suitable DSP Architecture for Efficient FPGA Implementation of FIR Filter

ECC:

14. A High-Speed FPGA Implementation of an RSD-Based ECC Processor

DCT:

15. A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT
16. Systolic Architecture Implementation of 1D DFT and 1D DCT
17. Performance Evaluation of an Integer Wavelet Transform for FPGA Implementation

**MEDIAN FILTER:**

18. A Low Energy 2D Adaptive Median Filter Hardware

**BIST:**

20. Preemptive Built-In Self-Test for In-Field Structural Testing

**NOC:**